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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,412	12/15/2003	Kwun-Yao Ho	JCLA10726	6310

7590 12/29/2005

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EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,412	HO ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *None*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 9-16 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention group, there being no allowable generic or linking claim. Applicant's election without traverse of group I, claims 1-8 and 17-24, in the reply filed on 15 December 2005 is acknowledged. Claims 9-16 are cancelled by the applicant. Claims 1-8 and 17-24 are considered in this Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 and 17-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Bindra et al. (US 5129142).

Regarding claim 1, as shown in figures 3B and 3C, Bindra et al. disclose a vertical routing structure for a multi-layered substrate with a lamination structure, wherein the lamination structure (conventionally laminated, see column 4, line 66 continuing column 5, line 2) has at least a through-hole linking the two surfaces of the lamination structure, the vertical routing structure comprising:

(a) A conductive rod 2 (a stud of joint metal, see column 5, lines 40-41) positioned inside the through-hole 8 (vias, see column 5, line 34) and both ends of the conductive rod protruding above the two surfaces (surfaces of dielectric layers 4, see column 5, lines 10-16) of the lamination structure respectively;

(b) a conductive layer (a thin electrically continuous metal layer, see column 4, lines 34-40) formed between the interior sidewall of the through-hole and the conductive rod.

Regarding claim 2, as clearly shown in figures 3B and 3C, Bindra et al. further disclose:

(a) A first mask layer (top dielectric layer 1) having at least a first opening (vias are opened up as shown in the figures, see abstract, line 4) on one surface (top surface) of the lamination structure;

(b) a second mask layer (bottom dielectric layer 1) having at least a second opening on another surface (bottom surface) of the lamination structure;

(c) the ends of the conductive rod not only fill up the first opening and the second opening but also protrude beyond the surfaces of the first mask layer and the second mask layer respectively.

It is noticed that Bindra et al. disclose an opened up vertical conductive vias structure. The structure has a wider opening on both ends of the conductive vias. As can be seen in the figures, each dielectric layer 1 has an opening wider than the diameter of the conductive via.

Regarding claim 3, as clearly shown in figures 3B and 3C, Bindra et al. disclose the second opening has a diameter greater than the through-hole (via 8).

Regarding claim 4, as clearly shown in figures 3B and 3C, Bindra et al. disclose one end of the conductive rods 2 serves as a bump 7 (contact lands, see column 5,line 35).

Regarding claim 5, as clearly shown in figures 3B and 3C, Bindra et al. further disclose a bump 7 attached to one end of the conductive rod.

Regarding claims 6 and 7, as shown in figure 3D, Bindra et al. disclose a pre-solder block 13 (solder paste or solder ball, see column 5, lines 48-49) attached to one end of the conductive rod 2. It is noticed that the land 7 is served as a joint for electrical connection to another substrate or a surface mounting chip, see column 4, line 66 continuing column 5, line 2.

Regarding claim 8, as shown in figure 1A, Bindra et al. disclose the lamination structure comprising at least a buried circuit layer 5 (signal lines, see column 5, line 16) that connects electrically with the conductive layer. It is noticed that conductive vias are conventionally known to electrically connect signal lines between different layers of a printed circuit board.

Regarding claim 17, Bindra et al. disclose every limitation as shown in claims 1 and 2 above.

Regarding claim 18, Bindra et al. disclose every limitation as shown in claim 3 above.

Regarding claim 19, as shown in figure 3A, Bindra et al. disclose an electrically continuing metal layer 9 (metallization) on the external surface of the vias 8 including the peripheral surface of the openings of the mask layers (the dielectric layers 1), see column 5, lines 29-55.

Regarding claim 20, Bindra et al. disclose every limitation as shown in claim 4 above.

Regarding claim 21, Bindra et al. disclose every limitation as shown in claim 5 above.

Regarding claim 22, Bindra et al. disclose every limitation as shown in claim 6 above.

Regarding claim 23, Bindra et al. disclose every limitation as shown in claim 7 above.

Regarding claim 24, Bindra et al. disclose every limitation as shown in claim 8 above.

Citation of Relevant Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kimura et al. (US 5286926) disclose an integrated circuit package and process for producing same.

Nakaso et al. (US 5444189) disclose a printed wiring board and production thereof.

Carpenter et al. (US 5495665) disclose a process for providing a landless via connection.

Sippel (US 5539181) discloses a circuit board.

Swamy (US 5541368) discloses a laminated multi chip module interconnect apparatus.

Tokuda et al. (US 5870289) disclose a chip connection structure having direct through-hole connections through adhesive film and wiring substrate.

Milkovich et al. (US 6399892) disclose a compensated chip interposer.

Curcio et al. (US 6465084) disclose a method and structure for producing Z-axis interconnection assembly of printed wiring board elements.

Sako (US 6486409) discloses a flexible wiring substrate.

Kobayashi et al. (US 6486414) disclose a through-hole structure and printed circuit board including the through-hole structure.

Muramatsu et al. (US 6730859) disclose a substrate for mounting electronic parts thereon and method of manufacturing same.

Higuchi et al. (US 6768064) disclose a multilayer wiring board assembly, multilayer wiring board assembly component and method of manufacture thereof.

Fuller et al. (US 6809269) disclose a circuitized substrate assembly and method of making same.

Shimizu et al. (US 6941648) disclose a method for producing printed wiring board.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

I.B Patel

Hoa C. Nguyen
22 December 2005

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Art Unit: 2841